興訊科技股份有限公司

文件封面履歷表

文 件 名 稱	apm6656-Shielding case 產品規格書 (**Preliminary** Production Information Data Sheet)	文 件 編 號	6656 Shielding case-C401

版本	發行日期	撰寫者/修改者	變更內容
A	2011.07.07	Brian Hu	新建(v0.1)(WIFI IC 6027 to 6030; copy from 6658/6659 datasheet rename to 6656) add WIFI FEATURE 1.SW AP 2. Wi-Fi Direct Need add 6656 picture, update WIFI test result
B	2012.05.16	杜顏彰	修改 2.1.1 原 **Windows Mobile 5.0 & 6.0**，刪除。 修改 2.2.2 原 Windows CE，刪除。(v0.2)
C	2014.07.16	Ryan Lee	更換主晶片（BC6 to BC8811）

核　　准	賴惠程	制 訂 人	Brian Hu	制 訂 單 位	研發處

發行蓋章處

表單編號：2Q0101A

apm6656 WiFi 802.11 b/g/n & BT4.0 Dual Mode Dual Radio Module

DESCRIPTION

With a small form factor of 9×11×1.55mm max., the apm6656 is a full-featured WiFi 802.11b/g/n & Bluetooth V4.0 Dual Mode module that simultaneously provides WiFi and Bluetooth connections.

By providing flexible host interfaces combined with support for embedded operating systems, the apm6656 enables rapid integration of WiFi and Bluetooth technology into a variety of host devices. The pre-tested and pre-certified module eliminates the need to create custom designs, resulting in greatly reduced development risk, costs, and time-to-market.

GENERAL FEATURES

- Small footprint: 9×11×1.55 mm max
- Support for state-of-the-art WiFi-Bluetooth co-existence and VoIP optimizations
- Support for single antenna configuration for WiFi and Bluetooth
- EEPROM and full RF front-end integrated for WiFi and Bluetooth
- External clock sharing for WiFi and Bluetooth
- Excellent GSM/GPRS/DCS/PCS/WCDMA/GPS radio coexistence
- Support for drivers on embedded OS
- RoHS compliant

WIFI FEATURES

- IEEE 802.11b/g/n compliant
- Host interface: SDIO 1-bit, SDIO 4-bit, SDIO SPI
- Support for WAPI security
- Supports Access Point tethering functionality (Soft AP for Linux and Android)
- Designed for Wi-Fi Direct™

BLUETOOTH FEATURES

- Dual-mode Bluetooth® /Bluetooth low energy radio
- Fully qualifiable Bluetooth v4.0 IC
- Can be used as part of a Bluetooth v4.0 + HS system
- High-speed UART port (up to 4Mbps)

APPLICATIONS

- Smart phone / PDA / PDA phone / WiFi phone / DSC / DVC with both WiFi and Bluetooth connectivity

APPEARANCE

PICTURE WAIT

REVISION HISTORY

Date	Release	Author	Description
2011.07.07	0.1	Brian Hu	Initial release
2012.05.16	0.2	Tu Yen Chang	Deleted Windows CE and Windows Mobile 5.0 & 6.0.
2014.07.16	0.3	Ryan Lee	Replacement of BT chip & To add 4 pins for NC terminal.(The 11th、12th、13th.、32th pins)

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Website: http://www.apmcomm.com – E-mail: sales@apmcomm.com

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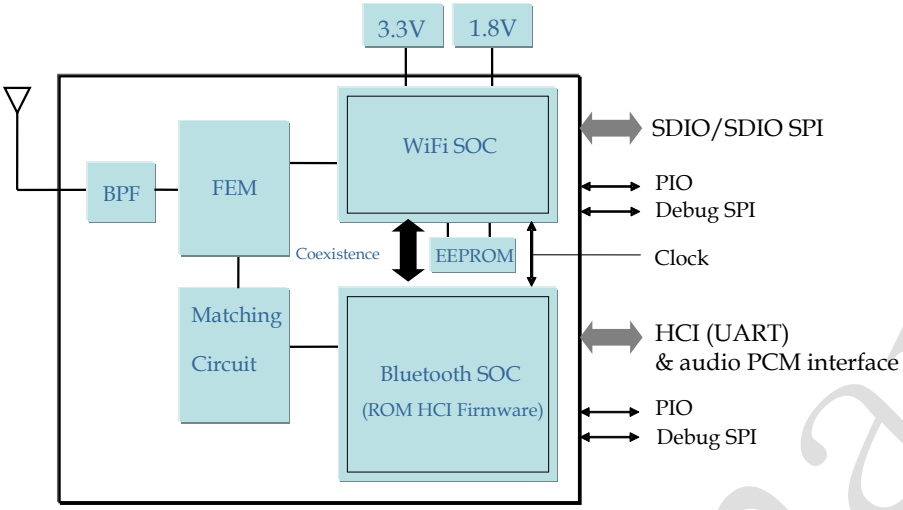
1 Hardware Specification

1-1 General Specification

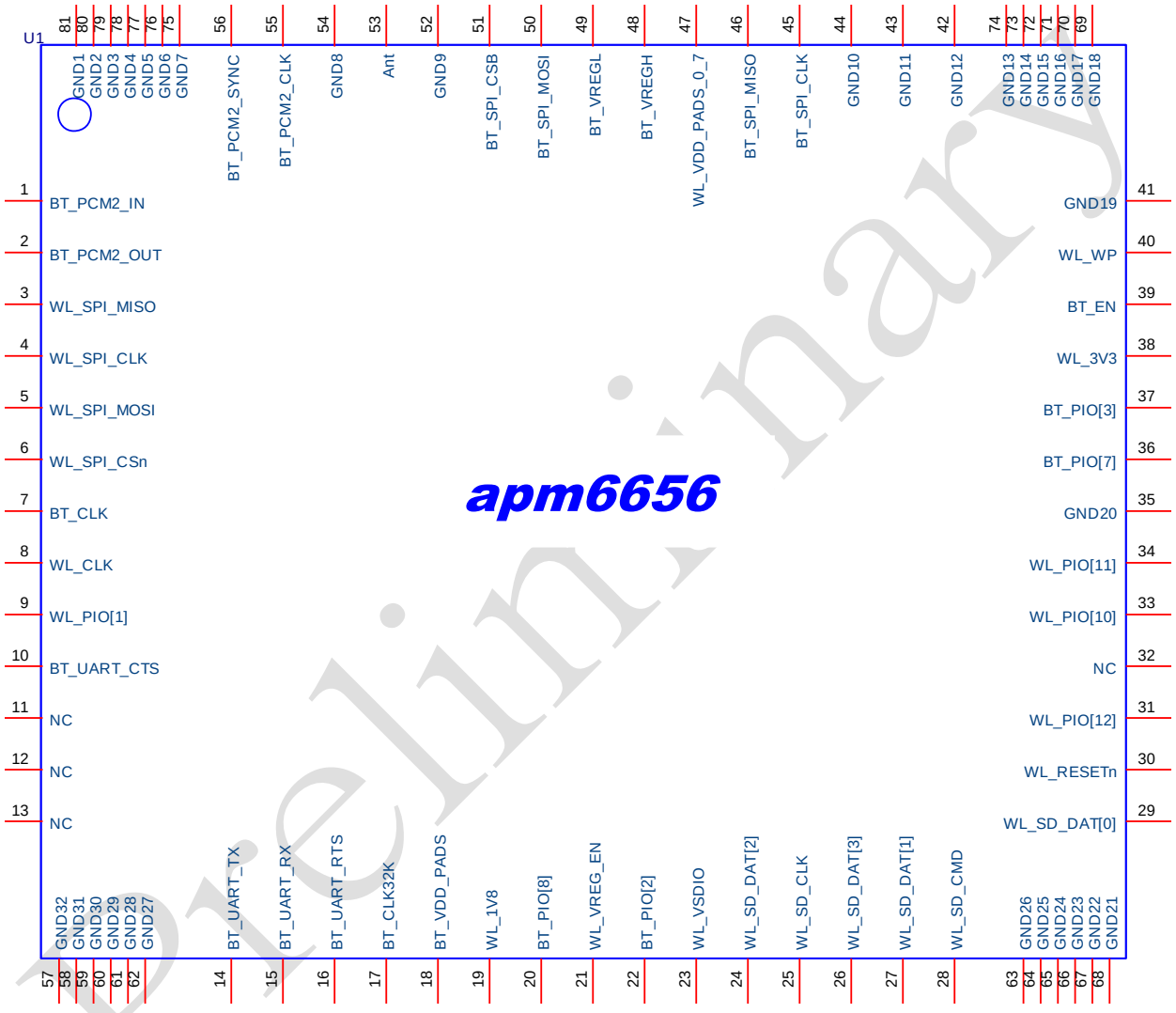
WiFi part:	
Network Standard	IEEE 802.11b/g/n Compliant
Host Interface	SDIO v2.0: SDIO 1-bit, SDIO 4-bit, SDIO SPI
Frequency Band	Channel 1 to 13
Data Transfer Mode	OFDM & DSSS
Modulation	64QAM (MCS0-7, 400/800ns 72.2, 65, 58.5, 57.8, 52, 43.3, 39, 28.9, 26, 21.7, 19.5, 14.4, 13, 7.2, 6.5Mbps), 64QAM (54, 48Mbps), 16QAM (36, 24Mbps), QPSK (18, 12Mbps), BPSK (9, 6Mbps); CCK (11, 5.5 Mbps), DQPSK (2 Mbps), DBPSK (1Mbps). STBC reception for MCS0-7
Access Method	Ad hoc mode, Infrastructure mode
Media Access Protocol	CSMA/ CA (Carrier Sense Multiple Access with Collision Avoidance)
Antenna	External single antenna support. The output impedance is 50Ω.
Bluetooth part:	
Bluetooth Specification	Dual-mode Bluetooth / Bluetooth low energy radio
Interface	UART(up to 4Mbps), SPI, PCM/I2S
Frequency Band	2400 to 2480MHz (79 channel) for basic rate & EDR 2400 to 2480MHz (40 channel) for BLE
Modulation	GFSK & $\pi/4$ DPSK & 8DPSK for basic rate & EDR GFSK for BLE
Antenna	External single antenna support. The output impedance is 50Ω.

1-1-1 Block Diagram



1-2 Pinout

1-2-1 Pin Assignment



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1-2-2 Pin Description

* I/O: Digital Input/Output, I: Digital Input, O: Digital Output, A: Analog, PU: Pull-up, PD: Pull-down

#	Name	I/O	Pin Status on Reset	Supply Domain	Description
1	BT_PCM2_IN	I	PD	BT_VDD_PADS	Synchronous data input
2	BT_PCM2_OUT	O	PD	BT_VDD_PADS	Synchronous data output
3	WL_SPI_MISO	O	PD	WL_VDD_PADS_0_7	Debug SPI data output
4	WL_SPI_CLK	I	PD	WL_VDD_PADS_0_7	Debug SPI clock
5	WL_SPI_MOSI	I	PD	WL_VDD_PADS_0_7	Debug SPI data input
6	WL_SPI_CSn	I	PU	WL_VDD_PADS_0_7	Debug SPI chip select, active low
7	BT_CLK	I	-	-	Clock input for BT
8	WL_CLK	I	-	-	Clock input for WiFi
9	WL_PIO[1]	I/O	-	WL_3V3	Programmable input/output
10	BT_UART_CTS	I/O	PU	BT_VDD_PADS	UART clear to send, active low
11	NC	-	-	-	-
12	NC	-	-	-	-
13	NC	-	-	-	-
14	BT_UART_TX	O	PU	BT_VDD_PADS	UART data output active high
15	BT_UART_RX	I	PU	BT_VDD_PADS	UART data input active high
16	BT_UART_RTS	O	PU	BT_VDD_PADS	UART request to send active low
17	BT_CLK32K	I	PD	BT_VDD_PADS	Dedicated 32kHz external reference clock input
18	BT_VDD_PADS	Power	-	-	Positive supply for all digital Input/Output ports, UART/SDIO ports, and PIO ports
19	WL_1V8	Power	-	-	Power supply for analogue/digital sections
20	BT_PIO[8]	I/O	-	BT_VDD_PADS	Programmable input/output
21	WL_VREG_EN	Power	PD	-	Enable for all regulators
22	BT_PIO[2]	I/O	-	BT_VDD_PADS	Programmable input/output
23	WL_VSDIO	Power	-	-	Positive supply for SDIO interface
24	WL_SD_DAT[2]	I/O	PU	WL_VSDIO	SDIO bidirectional data line (not used in CSPI mode)
25	WL_SD_CLK	I	PU	WL_VSDIO	SDIO or CSPI clock line
26	WL_SD_DAT[3]	I/O	PU	WL_VSDIO	SDIO bidirectional data line or CSPI chip select

#	Name	I/O	Pin Status on Reset	Supply Domain	Description
27	WL_SD_DAT[1]	I/O	PU	WL_VSDIO	SDIO bidirectional data line or CSPI interrupt
28	WL_SD_CMD	I	PU	WL_VSDIO	SDIO bidirectional command line or CSPI MOSI
29	WL_SD_DAT[0]	I/O	PU	WL_VSDIO	SDIO bidirectional data line or CSPI MISO
30	WL_RESETn	I	PU	WL_RESETB	Reset, active low
31	WL_PIO[12]	I/O	-	WL_3V3	Programmable input/output
32	NC	-	-	-	-
33	WL_PIO[10]	I/O	-	WL_3V3	Programmable input/output
34	WL_PIO[11]	I/O	-	WL_3V3	Programmable input/output
35	GND	GND	-	-	Ground
36	BT_PIO[7]	I/O	PD	BT_VDD_PADS	Programmable input/output
37	BT_PIO[3]	I/O	PD	BT_VDD_PADS	Programmable input/output
38	WL_3V3	Power	-	-	Positive supply for AIO[0]-AIO[3] , PIO[8]-PIO[15], and FEM
39	BT_EN	I	-	BT_VDD_PADS	Chip enable
40	WL_WP	I	-	-	Write protection for internal EEPROM
41	GND	GND	-	-	Ground
42	GND	GND	-	-	Ground
43	GND	GND	-	-	Ground
44	GND	GND	-	-	Ground
45	BT_SPI_CLK	I	PD	BT_VDD_PADS	SPI clock
46	BT_SPI_MISO	O	PD	BT_VDD_PADS	SPI data output
47	WL_VDD_PADS_0_7	Power	-	-	Positive supply for Debug SPI, PIO[0]-PIO[7]
48	BT_VREGH	Power	-	-	High regulator input
49	BT_VREGL	Power	-	-	High regulator output and low regulator input
50	BT_SPI_MOSI	I	PD	BT_VDD_PADS	SPI data input
51	BT_SPI_CSB	I	PD	BT_VDD_PADS	Chip select for Serial Peripheral Interface, active low
52	GND	GND	-	-	Ground
53	ANT	A	-	-	RF input/output
54	GND	GND	-	-	Ground
55	BT_PCM2_CLK	I/O	PD	BT_VDD_PADS	Synchronous data clock

#	Name	I/O	Pin Status on Reset	Supply Domain	Description
56	BT_PCM2_SYNC	I/O	PD	BT_VDD_PADS	Synchronous data sync

All the big pads on the bottom of the module should be tied to ground.

1-3 WiFi Pins

1-3-1 SDIO Pins

apm6656 supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access apm6656.

The SDIO bus has weak internal pull up resistors on chip.

SDIO Bus Name	Pin #	Pin Name	SD 1-bit Mode	SD 4-bit Mode
DAT3	26	WL_SD_DAT[3]	SD ：Card detect	DAT[3]/CD :Data line 1 or card detect
DAT2	24	WL_SD_DAT[2]	RW: Read wait	DAT[2]/RW :Data line 1 or read wait
DAT1	27	WL_SD_DAT[1]	IRQ#: Interrupt	DAT[1]/IRQ# :Data line 1 or interrupt
DAT0	29	WL_SD_DAT[0]	DATA: Data line	DAT[0]: Data line 0
CMD	28	WL_SD_CMD	CMD: Command line	CMD: Command line
CLK	25	WL_SD_CLK	CLK: Clock	CLK: Clock

1-3-2 CSPI Pins

While SDIO port is not available on host platform, apm6656 supports a SD-SPI device interface that connects to Synchronous Serial Port (SSP) pins.

The SD-SPI bus has weak internal pull up resistors on chip.

SD-SPI Name	Pin #	Pin Name	Description
CS	26	WL_SD_DAT[3]	Card Select
IRQ	27	WL_SD_DAT[1]	Interrupt
DO	29	WL_SD_DAT[0]	MISO：Data output
DI	28	WL_SD_CMD	MOSI：Data input
SCLK	25	WL_SD_CLK	Clock

1-3-3 Debug SPI Pins

apm6656 has a SPI interface for test and debugging purposes. The lab tools, such as UniTest and UniPSUtil, can communicate with apm6656 WiFi part using the SPI protocol over a connection to an LPT port.

Debug SPI Name	Pin #	Pin Name	Description
MISO	3	WL_SPI_MISO	Debug SPI data output
MOSI	5	WL_SPI_MOSI	Debug SPI data input
CLK	4	WL_SPI_CLK	Debug SPI clock
CSn	6	WL_SPI_CSn	Debug SPI chip select, active low
VDDIO	47	WL_VDD_PADS_0_7	Serial I/O VDD

1-3-4 PIO Pins

The PIO pins are used to implement user defined input and output signals to and from the module such as external interrupts, LED controlled outputs, and other user-defined I/Os. Each PIO can be independently controlled.

- WL_PIO[11:10]: LED WLAN link activities.
- WL_PIO[12]: Host wakeup.
- WL_PIO[1]: WiFi External clock request out
- Other PIOs: Reserved

1-3-5 WP Pin

WL_WP is write protection for internal EEPROM. The internal EEPROM stores calibration table, MAC address, etc. for WiFi part. When the pin is pulled high, it protects the EEPROM content. If tied to VSS, normal memory read/write operation is enabled.

The WiFi firmware does not incorporate any support for writing to the EEPROM during normal operation. This significantly reduces the risk of spurious writes corrupting the contents of the EEPROM, and means it is not possible to repair any damage that may occur. Hence, it is suggested that keep the pin, WL_WP, permanently pulled high to minimize the risk of data corruption.

1-3-6 Power Pins

The following list shows the pins referenced to WL_VSDIO.

Pin #	Pin name	Pin #	Pin name	Pin #	Pin name
24	WL_SD_DAT[2]	25	WL_SD_CLK	26	WL_SD_DAT[3]
27	WL_SD_DAT[1]	28	WL_SD_CMD	29	WL_SD_DAT[0]

The following list shows the pins referenced to WL_VDD_PADS_0_7.

Pin #	Pin name	Pin #	Pin name	Pin #	Pin name
3	WL_SPI_MISO	4	WL_SPI_CLK	5	WL_SPI_MOSI
6	WL_SPI_CSn	30	WL_RESETn		

The following list shows the pins referenced to WL_3V3.

Pin #	Pin name	Pin #	Pin name	Pin #	Pin name
9	WL_PIO[1]	33	WL_PIO[10]	34	WL_PIO[11]
31	WL_PIO[12]				

*WL_VDD_PADS_0_7 voltage power level must be the same as BT_VDD_PADS and the oscillator.

1-4 Bluetooth Pins

1-4-1 UART Pins

apm6656 supports a Universal Asynchronous Receiver Transmitter (UART) interface with programmable baud rate up to 4Mbps. BlueCore Serial Protocol (BCSP), a proprietary alternative to the standard Bluetooth UART Host Transport, is also supported.

UART Bus Name	Pin #	Pin Name	Description
CTS	10	BT_UART_CTS	UART clear to send active low
RTS	16	BT_UART_RTS	UART request to send active low
TX	14	BT_UART_TX	UART data output active high
RX	15	BT_UART_RX	UART data input active high
VDDIO	18	BT_VDD_PADS	Serial I/O VDD

1-4-2 PCM Pins

apm6656 audio Pulse Code Modulation (PCM) interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth. The Digital Audio Interface (I2S) shares the same pins as the PCM interface.

Bus Name	Pin #	Pin Name	Description
SYNC	56	BT_PCM2_SYNC	PCM: PCM2 Synchronous data sync I2S: I2S_WS
CLK	55	BT_PCM2_CLK	PCM: PCM2 Synchronous data clock I2S: I2S_SCK
OUT	2	BT_PCM2_OUT	PCM: PCM2 Synchronous data output I2S: I2S_OUT
IN	1	BT_PCM2_IN	PCM: PCM2 Synchronous data input I2S: I2S_IN
VDDIO	18	BT_VDD_PADS	Serial I/O VDD

PCM2/I2S interface mapping

1-4-3 Debug SPI Pins

apm6656 has a SPI interface for debug primarily. The lab tools, PSTOOL, can communicate with apm6656 BT part using the SPI protocol over a connection to an LPT port.

Debug SPI Name	Pin #	Pin Name	Description
MISO	46	BT_SPI_MISO	Debug SPI data output
MOSI	50	BT_SPI_MOSI	Debug SPI data input
CLK	45	BT_SPI_CLK	Debug SPI clock
CS	51	BT_SPI_CSB	Debug SPI chip select, active low
VDDIO	18	BT_VDD_PADS	Serial I/O VDD

1-4-4 PIO Pins

The PIO pins are used to implement user defined input and output signals to and from the module such as external

interrupts, LED controlled output and other user-defined I/Os. Each PIO can be independently controlled.

- BT_PIO[7]: LED Bluetooth TX activities.
- BT_PIO[2]: Bluetooth external clock request out.
- BT_PIO[3]: Bluetooth external clock request in.
- BT_PIO[8]: LED Bluetooth RX activities.

1-4-5 Power Pins

The following list shows the pins referenced to BT_VDD_PADS.

Pin #	Pin name	Pin #	Pin name	Pin #	Pin name
1	BT_PCM2_IN	22	BT_PIO[2]	55	BT_PCM2_CLK
2	BT_PCM2_OUT	36	BT_PIO[7]	56	BT_PCM2_SYNC
10	BT_UART_CTS	37	BT_PIO[3]		
14	BT_UART_TX	39	BT_EN		
15	BT_UART_RX	45	BT_SPI_CLK		
16	BT_UART_RTS	46	BT_SPI_MISO		
17	BT_CLK32K	50	BT_SPI_MOSI		
20	BT_PIO[8]	51	BT_SPI_CSB		

*BT_VDD_PADS voltage power level must be the same as WL_VDD_PADS_0_7

1-5 External Voltage Source

The external supply rails to apm6656 should have less than 10mV rms noise levels between 0 to 10 MHz. Single tone frequencies are also to be avoided.

Transient response of external regulators used should be <= 5us for WiFi and <= 20us for Bluetooth, respectively.

Supply voltage range	
1.8V	1.8V+/- 5% (ripple Vpp<10mV rms)
3.3V	3.3V +/-5% (ripple Vpp<10mV rms)

1-5-1 WiFi Reset

WL_RESETn is an active low reset input that is internally filtered using the internal low frequency clock oscillator to avoid spurious resets. A reset occurs after the signal has been asserted for between 250 and 375us. This pin may be tied to WL_VDD_PADS_0_7 if unused; otherwise it should be asserted for at least 1ms to force a reset.

The power supply supervisor monitors WL_VDD_CORE (internal module voltage) to trigger a power-on-reset. This occurs when the supply falls below 1.05V (typical) in normal operation or 0.825V (typical) in deep sleep, and ends when the supply exceeds 1.10V (typical). Glitches of up to 30mV and 2.5us duration, which could be caused by large load steps, will not trigger a reset.

Each of the internal processors has its own independent watchdog timer to detect and recover from erroneous software operation. These are typically configured with a timeout of 1.5s, but this may be increased up to a maximum of 64s for reduced power consumption. The watchdogs are enabled at power-on and continue operating while WiFi is in deep sleep.

During all forms of reset most digital I/O pins (including both bidirectional pins and dedicated inputs or outputs) default to high impedance with weak internal pull-downs. The only exceptions are WL_RESETn and WL_SPI_CS which both have pull-ups, and the SDIO/CSPI bus which is on an independent reset domain. The SDIO/CSPI host interface is only fully reset by the WL_RESETn pin or the power supply supervisor; other forms of reset leave the host interface initialized but simply clear the I/O Enable bit for function 1.

Following a reset, WiFi automatically generates safe clocks for internal use. If an external reference clock is connected to WL_CLK then this is assumed to be at the maximum supported frequency, otherwise the PLL free runs at a nominal frequency. In either case the generated clock will be slower than in normal operation, but this is sufficient for safely booting and configuring the IC.

Power-on Reset	Min	Typ	Max	Units
Reset release on WL_VDD_DIG rising (HI)	1.030	-	1.150	V
Reset assert on WL_VDD_DIG falling (LO)	HI-0.060	-	HI-0.045	V
Reset assert on WL_VDD_DIG falling (Sleep mode)	0.770	0.785	0.800	V

1-5-2 Bluetooth Reset

The APM6656 the reset function is internally tied to the BT_EN pin. The BT_EN pin is an active low reset. To ensure a full reset the reset signal should be asserted for a period greater than 5ms.

A warm reset function is also available under software control. After a warm reset the RAM data remains available.

1-5-3 WiFi Clock

The external reference clock is applied to the apm6656 WL_CLK input pin. This signal should meet the specifications outlined in the table below. The default WiFi clock in the module is set as 26MHz. We recommended customer to design with 26MHz OSC to prevent inconvenience.

Supported Parameter		Min	Typ	Max	Unit
Frequency		19.2	26	40	MHz
Frequency tolerance		-20	-	+20	ppm
Duty cycle		40:60	50:50	60:40	%
Edge jitter		-	-	1.6	ps rms
Signal level	AC couple	400	500	750	mV pk-pk

1-5-4 BT Clock

The external reference clock is applied to the apm6656 BT_CLK input pin. This signal should meet the specifications outlined in the table below. The default BT clock in the module is set as 26MHz. We recommended customer to design with 26MHz OSC to prevent inconvenience.

Supported Parameter		Min	Typ	Max	Unit
Frequency		19.2	26	40	MHz
Frequency tolerance		-20	-	+20	ppm
Duty cycle		40:60	50:50	60:40	%
Edge jitter		-	-	1.6	ps rms
Signal level	AC coupled	400	500	750	mV pk-pk

1-5-5 BT Sleep Clock

The sleep clock is an external 32.768kHz clock for deep sleep and other low-power modes. This signal should meet the specifications outlined in the table below.

Note：Sleep clock can be input on BT_CLK32K Pin.

Supported Parameter		Min	Typ	Max	Unit
Frequency		32.748	32.768	32.788	KHz
Frequency tolerance		-25	-	+25	ppm
Duty cycle		40:60	50:50	60:40	%
Edge jitter		-	-	10	ns rms
Signal level	VIL	-0.4	-	+0.4	V
	VIH	0.8* BT_VDD_PADS	-	BT_VDD_PADS+0.3	

1-6 Electrical Specifications

1-6-1 Absolute Maximum Rating

Symbol	Description	Min.	Max.	Units
T_{ST}	Storage temperature	-30	+85	℃
WL_3V3	Positive supply for AIO[0]-AIO[3] , PIO[8]-PIO[15], and FEM	+1.7	+3.6	V
WL_1V8	Power supply for VDD_REG_IN_ANA, VDD_REG_IN_DIG.	+1.45	+2.0	V
WL_VREG_EN	Enable for WiFi linear regulators	-0.4	+2.0	V
WL_VDD_PADS_0_7	Power supply for SPI, EEPROM, RST#, EEPROM and PIO[0]-PIO[7]	+1.7	+3.6	V
WL_VSDIO	Positive supply for SDIO interface	+1.7	+3.6	V
BT_VREGH	High regulator input	+2.3	+4.8	V
BT_VREGL	High regulator output and low regulator input	+1.7	+2.0	V
BT_VDD_PADS	Positive supply for digital input/output ports	+1.2	+3.6	V
BT_EN	Take high to enable BT regulator	+1.2	+3.6	V

*Absolute maximum ratings indicate limits beyond which damage to the device may occur.

1-6-2 Recommended Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Units
T_{OP}	Operating temperature	-20	+25	+70	℃
WL_3V3	Positive supply for AIO[0]-AIO[3] , PIO[8]-PIO[15], and FEM	+3.0	+3.3	+3.6	V
WL_1V8	Power supply for VDD_REG_IN_ANA, VDD_REG_IN_DIG.	+1.7	+1.8	+2.0	V
WL_VREG_EN	Enable for WiFi voltage regulators	+1.7	+1.8	+2.0	V
WL_VDD_PADS_0_7	Power supply for SPI, RST#, and PIO[0]-PIO[7]	+1.7	+1.8/+3.3	+3.3	V
WL_VSDIO	Positive supply for SDIO interface	+1.7	+1.8/+3.3	+3.6	V
BT_VREGH	High regulator input	+3.0	+3.3	+3.6	V
BT_VREGL	High regulator output and low regulator input	+1.7	+1.8	+1.9	V
BT_VDD_PADS	Positive supply for digital I/O ports	+1.7	+1.8/+3.3	+3.6	V
BT_EN	Take high to enable BT regulator	+1.7	+3.3	+3.6	V

1-7 Current Consumption

1-7-1 WLAN Current Consumption

Conditions: WL_1V8= WL_VREG_EN= +1.8V, WL_3V3= WL_VDD_PADS_0_7= WL_VSDIO= +3.3 V, T_{OP}= 25°C

Parameter	Test conditions	Units	Min.	Typ.	Max.
802.11b Current Consumption					
11Mbps transmit@+17dBm	Continuous packet, PSDU length of 1024 Bytes (958us), packet interval 50µs	mA	-	221/ 3V3 120/ 1V8	-
11Mbps receive	-85dBm.Continuous packet, PSDU length of 1024 Bytes, packet interval 50µs	mA	-	10/ 3V3 133/ 1V8	-
802.11g Current Consumption					
54Mbps transmit@+15dBm	Continuous packet, PSDU length of 1024 Bytes (179us), packet interval 117µs	mA	-	123/ 3V3 127/ 1V8	-
54Mbps receive	-70dBm. Continuous packet, PSDU length of 1024 Bytes, packet interval 50µs	mA	-	10/ 3V3 141 /1V8	-
802.11n Current Consumption					
MCS7 transmit@+13dBm	Continuous packet, PSDU length of 4096 Bytes	mA	-	120/ 3V3 130/ 1V8	-
MCS7 receive	-68dBm. Continuous packet, PSDU length of 4096 Bytes	mA	-	10/ 3V3 130/ 1V8	-
Listen	Receive but no OFDM/CCK packet in air	mA	-	10/3V3 140/1V8	-
Sleep Current Consumption					
Deep sleep		uA	-	13/3V3 75/1V8	-

***The WIFI current is preliminary value**

1-7-2 Bluetooth Current Consumption

Conditions: BT_VREGH= BT_VDD_PADS= BT_EN= +3.3V, BT_VREGL = NL, T_{OP}= 25°C

Parameter	Test conditions	Units	Min	Typ	Max
Current Consumption					
ACL no traffic	Master	mA	-	4.3	-
ACL with file transfer	Master	mA	-	6.7	-
ACL no traffic	Slave	mA	-	9.6	-
ACL with file transfer	Slave	mA	-	20.8	-
SCO HV1	Master	mA	-	34	-
SCO HV3	Master	mA	-	13.1	-
SCO HV1	Slave	mA	-	35.4	-
SCO HV3	Slave	mA	-	16.1	-
Inquire mode	Master	mA	-	24.4	-
Standby with host connection	Master	uA	-	45	-
Deep sleep with host connection	Master	uA	-	175	-

***The BT current is preliminary value**

1-8 RF Specification

1-8-1 WiFi RF Specification

Conditions: WL_1V8= WL_VREG_EN= +1.8V, WL_3V3= WL_VDD_PADS_0_7= WL_VSDIO= +3.3 V, T_{OP}= 25°C

Parameter	Test conditions	Units	Min.	Typ.	Max.
802.11b Transmit					
Operating frequency range		-	Ch 1	-	Ch 13
Transmit output power	1/2/5.5/11Mbps	dBm	15.5	+17	18.5
Center frequency tolerance		ppm	-	+5	-
ACPR: 1st side lobe power	Pout=+17.0dBm, 1/2/5.5/11Mbps	dBc	-	-42	-
ACPR: 2nd side lobe power	Pout=+17.0dBm, 1/2/5.5/11Mbps	dBc	-	-58	-
Transmit EVM	11Mbps, Channel 1~13	%	-	8	-
Transmit ramp-up time	10% ~ 90%	µs	-	0.8	-
Transmit ramp-down time	10% ~ 90%	µs	-	1	-
802.11b Receive					
Minimum input level sensitivity	11Mbps CCK, FER<8% at PSDU length of 1024 bytes	dBm	-	-85	-
Maximum input level capability	11Mbps CCK, FER<8% at PSDU length of 1024 bytes	dBm	-	+5	-
802.11g Transmit					
Operating frequency range		-	Ch 1	-	Ch 13
Transmit output power	54Mbps OFDM	dBm	13.5	+15	16.5
Center frequency tolerance	54Mbps OFDM	ppm	-	+5	-
Symbol clock freq. tolerance	54Mbps OFDM	ppm	-	+4	-
Transmit EVM	54Mbps OFDM, Channel 1~13	dB	-	-	-25
Transmit ramp-up time	10% ~ 90%	µs	-	0.8	-
Transmit ramp-down time	10% ~ 90%	µs	-	1	-
802.11g Receive					
Receive minimum input level sensitivity	54Mbps OFDM, FER<10% at PSDU length of 1024 bytes	dBm	-	-70	-
Receive maximum input level capability	54Mbps OFDM, FER<10% at PSDU length of 1024 bytes	dBm	-	-13	-

Parameter	Test conditions	Units	Min.	Typ.	Max.
802.11n 20MHz Transmit					
Operating frequency range		-	Ch 1	-	Ch 13
Transmit output power	MCS7	dBm	11	+12.5	14
Transmit EVM	65Mbps, Channel 1~13	dB	-	-	-28
Symbol clock frequency tolerance	MSC7	ppm	-	+5	-
Transmit center frequency tolerance	MCS7	ppm	-	+2	-
Spectrum Mask	f < fc-30, fc+30 <f	dBr	-	-49	-
	fc-30 <f <fc-20, fc+20 <f <fc+30	dBr		-42	
	fc-20 <f <fc-11, fc+11 <f <fc+20	dBr	-	-31	-
	fc-11 <f <fc-9, fc+9 <f <fc+11	dBr	-	-15	-
802.11n 20MHz Receive					
Receive minimum input level sensitivity	MCS7 (FER<10% at PSDU length of 1024 bytes)	dBm	-	-67	-
Receive maximum input level capability	MSC7 (FER<10% at PSDU length of 1024 bytes)	dBm	-	-17	-

1-8-2 Bluetooth RF Specification

Conditions: BT_VREGH= BT_VDD_PADS= BT_EN= +3.3V, BT_VREGL = NL, T_{OP}= 25°C

■ **Channel 0 (2402MHz)**

Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Basic Data Rate - Transmitter Test						
Maximum RF transmit power *(a)		4	5.5	7	Class1: 0 to +20 Class2: -6 to +4	dBm
Power Control Step		-	-	7	2 to 8	dB
Modulation Characteristic	Modulation index: Δf1avg	145	164	175	140 ≤ Δf1avg ≤ 175	kHz
	Modulation index: Δf2 avg	115	142	-	≥ 115	kHz
	Modulation index: Δf2avg / Δf1avg	0.8	0.93	-	≥ 0.8	NA
Initial carrier frequency tolerance		-35	+8.2	35	± 35	kHz
Carrier frequency drift rate		-20	+10	20	± 20	kHz/50us
Carrier frequency drift: one slot packet		-25	-8	25	± 25	kHz
Carrier frequency drift: three slot packet		-40	-7	40	± 40	kHz
Carrier frequency drift: five slot packet		-40	-9	40	± 40	kHz
Basic Data Rate - Receiver Test						
Sensitivity – single slot packets		-	-81	-70	≤ -70	dBm
Sensitivity – multi slot packets		-	-76	-70	≤ -70	dBm
Enhanced Data Rate – Transmitter Test						
Relative transmit power		-	-1.03	-	-4 to +1	dB
π/4 DQPSK Max carrier frequency stability ω_i		-75	2.7	75	≤ ±75 for all packets	kHz
π/4 DQPSK Max carrier frequency stability ω_o		-10	-1.9	10	≤ ±10 for all blocks	kHz
π/4 DQPSK Max carrier frequency stability $\lvert \omega_o+\omega_i \rvert$		-75	3.7	75	≤ ±75 for all blocks	kHz
8 DPSK Max carrier frequency stability ω_i		-75	3.1	75	≤ ±75 for all packets	kHz
8 DPSK		-10	-1.7	10	≤ ±10	kHz

Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Max carrier frequency stability ω_o					for all blocks	
8 DPSK Max carrier frequency stability | $\omega_o+\omega_i$ |		-75	3.6	75	≤ ±75 for all blocks	kHz
π/4 DQPSK Modulation Accuracy	rms DEVM	-	7.7	20	≤20	%
	99% DEVM	-	0	0.3	≤0.3	-
	Peak DEVM	-	21	35	≤35	%
8 DPSK Modulation Accuracy	rms DEVM	-	7.2	13	≤13	%
	99% DEVM	-	0	0.2	≤0.2	-
	Peak DEVM	-	18.1	25	≤25	%
EDR Differential Phase Encoding		-	100	-	99	%
Enhanced Data Rate – Receiver Test						
Sensitivity at 0.01% BER	π/4 DQPSK	-	-82.5	-70	≤-70	dBm
	8 DPSK	-	-73.5	-70	≤-70	
EDR Floor Performance		-	0	-	7.00E-006 1.00E-005	
EDR MAX input power			0		1.00E-003	
*(a) RF TX Power can be set by PSR setting.						
Low Energy - Transmitter Test (Channel 0_2402MHz)						
Maximum RF transmit power *(a)		4	5.5	7	< 10	dBm
Modulation Characteristic	Modulation index: Δf1avg	225	264	-275	225 ≤ Δf1avg ≤ 275	kHz
	Modulation index: Δf2 avg	185	229	-	≥ 185	kHz
	Modulation index: Δf2avg / Δf1avg	0.8	0.85	-	≥ 0.8	NA
Initial carrier frequency tolerance		-40	+2.4	40	± 40	kHz
Carrier frequency drift rate		-20	+7.3	20	± 20	kHz/50us
Carrier frequency drift: Max Drift		50	7	-	≤50	kHz
Low Energy – Receiver Test (Channel 0_2402MHz)						
Receiver sensitivity		-	-80	-70	≤-70	dBm
Receiver sensitivity - Frame Error Rate		-	0	30.8	≤30.8	%
PER Report Integrity - Frame Error Rate		50	50	65.4	50.0 ≤ PER ≤ 65.4	%

■ **Channel 39 (2441MHz)**

Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Basic Data Rate - Transmitter Test						
Maximum RF transmit power *(a)		4.5	6	7.5	Class1: 0 to +20 Class2: -6 to +4	dBm
Power Control Step		-	-	7	2 to 8	dB
Modulation Characteristic	Modulation index: Δf1avg	145	164.9	175	140 ≤ Δf1avg ≤ 175	kHz
	Modulation index: Δf2 avg	115	146.7	-	≥ 115	kHz
	Modulation index: Δf2avg / Δf1avg	0.8	0.88	-	≥ 0.8	NA
Initial carrier frequency tolerance		-35	+9.1	35	± 35	kHz
Carrier frequency drift rate		-20	-9.	20	± 20	kHz/50us
Carrier frequency drift: one slot packet		-25	-4.3	25	± 25	kHz
Carrier frequency drift: three slot packet		-40	+6.6	40	± 40	kHz
Carrier frequency drift: five slot packet		-40	-8.4	40	± 40	kHz
Basic Data Rate - Receiver Test						
Sensitivity – single slot packets		-	-81	-70	≤ -70	dBm
Sensitivity – multi slot packets		-	-76	-70	≤ -70	dBm
Enhanced Data Rate – Transmitter Test						
Relative transmit power		-	-1.01	-	-4 to +1	dB
π/4 DQPSK Max carrier frequency stability ω_i		-75	+4.2	75	≤ ±75 for all packets	kHz
π/4 DQPSK Max carrier frequency stability ω_o		-10	+1.6	10	≤ ±10 for all blocks	kHz
π/4 DQPSK Max carrier frequency stability $\lvert \omega_o+\omega_i \rvert$		-75	+4.7	75	≤ ±75 for all blocks	kHz
8 DPSK Max carrier frequency stability ω_i		-75	+4.1	75	≤ ±75 for all packets	kHz
8 DPSK Max carrier frequency stability ω_o		-10	+1.3	10	≤ ±10 for all blocks	kHz
8 DPSK Max carrier frequency stability $\lvert \omega_o+\omega_i \rvert$		-75	+4.8	75	≤ ±75 for all blocks	kHz

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Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
π/4 DQPSK Modulation Accuracy	rms DEVM	-	7.1	20	≤20	%
	99% DEVM	-	0	0.3	≤0.3	-
	Peak DEVM	-	19.5	35	≤35	%
8 DPSK Modulation Accuracy	rms DEVM	-	6.9	13	≤13	%
	99% DEVM	-	0	0.2	≤0.2	-
	Peak DEVM	-	18.5	25	≤25	%
EDR Differential Phase Encoding		-	100	-	99	%
Enhanced Data Rate – Receiver Test						
Sensitivity at 0.01% BER	π/4 DQPSK	-	-82.5	-70	≤-70	dBm
	8 DPSK	-	-73.5	-70	≤-70	
EDR Floor Performance		-	0	-	7.00E-006 1.00E-005	
EDR MAX input power			0		1.00E-003	
*(a) RF TX Power can be set by PSR setting.						
Low Energy - Transmitter Test (Channel 18_2442MHz)						
Maximum RF transmit power *(a)		4.5	6	7.5	< 10	dBm
Modulation Characteristic	Modulation index: Δf1avg	225	265.2	-275	225 ≤ Δf1avg ≤ 275	kHz
	Modulation index: Δf2 avg	185	224.2	-	≥ 185	kHz
	Modulation index: Δf2avg / Δf1avg	0.8	0.84	-	≥ 0.8	NA
Initial carrier frequency tolerance		-40	+3.9	40	± 40	kHz
Carrier frequency drift rate		-20	-4.3	20	± 20	kHz/50us
Carrier frequency drift: Max Drift		50	7	-	≤50	kHz
Low Energy – Receiver Test (Channel 18_2442MHz)						
Receiver sensitivity		-	-80	-70	≤-70	dBm
Receiver sensitivity - Frame Error Rate		-	0	30.8	≤30.8	%
PER Report Integrity - Frame Error Rate		50	50	65.4	50.0 ≤ PER ≤ 65.4	%

■ **Channel 79 (2480MHz)**

Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Basic Data Rate - Transmitter Test						
Maximum RF transmit power *(a)		4.5	6	7.5	Class1: 0 to +20 Class2: -6 to +4	dBm
Power Control Step		-	-	7	2 to 8	dB
Modulation Characteristic	Modulation index: Δf1avg	145	165.5	175	140 ≤ Δf1avg ≤ 175	kHz
	Modulation index: Δf2 avg	115	146	-	≥ 115	kHz
	Modulation index: Δf2avg / Δf1avg	0.8	0.88	-	≥ 0.8	NA
Initial carrier frequency tolerance		-35	+7.8	35	± 35	kHz
Carrier frequency drift rate		-20	-10	20	± 20	kHz/50us
Carrier frequency drift: one slot packet		-25	-6.8	25	± 25	kHz
Carrier frequency drift: three slot packet		-40	-6.7	40	± 40	kHz
Carrier frequency drift: five slot packet		-40	-6.8	40	± 40	kHz
Basic Data Rate - Receiver Test						
Sensitivity – single slot packets		-	-81	-70	≤ -70	dBm
Sensitivity – multi slot packets		-	-76	-70	≤ -70	dBm
Enhanced Data Rate – Transmitter Test						
Relative transmit power		-	-0.99	-	-4 to +1	dB
π/4 DQPSK Max carrier frequency stability ω_i		-75	+3.7	75	≤ ±75 for all packets	kHz
π/4 DQPSK Max carrier frequency stability ω_o		-10	+2	10	≤ ±10 for all blocks	kHz
π/4 DQPSK Max carrier frequency stability $\lvert \omega_o+\omega_i \rvert$		-75	+4.8	75	≤ ±75 for all blocks	kHz
8 DPSK Max carrier frequency stability ω_i		-75	+4.4	75	≤ ±75 for all packets	kHz
8 DPSK Max carrier frequency stability ω_o		-10	-1.7	10	≤ ±10 for all blocks	kHz
8 DPSK Max carrier frequency stability $\lvert \omega_o+\omega_i \rvert$		-75	+4.8	75	≤ ±75 for all blocks	kHz

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Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
π/4 DQPSK Modulation Accuracy	rms DEVM	-	8.1	20	≤20	%
	99% DEVM	-	0	0.3	≤0.3	-
	Peak DEVM	-	22.8	35	≤35	%
8 DPSK Modulation Accuracy	rms DEVM	-	7.8	13	≤13	%
	99% DEVM	-	0	0.2	≤0.2	-
	Peak DEVM	-	20.5	25	≤25	%
EDR Differential Phase Encoding		-	100	-	99	%
Enhanced Data Rate – Receiver Test						
Sensitivity at 0.01% BER	π/4 DQPSK	-	-82.5	-70	≤-70	dBm
	8 DPSK	-	-73.5	-70	≤-70	
EDR Floor Performance		-	0	-	7.00E-006 1.00E-005	
EDR MAX input power			0		1.00E-003	
*(a) RF TX Power can be set by PSR setting.						
Low Energy - Transmitter Test (Channel 39_2480MHz)						
Maximum RF transmit power *(a)		4.5	6	7.5	< 10	dBm
Modulation Characteristic	Modulation index: Δf1avg	225	264.5	-275	225 ≤ Δf1avg ≤ 275	kHz
	Modulation index: Δf2 avg	185	222	-	≥ 185	kHz
	Modulation index: Δf2avg / Δf1avg	0.8	0.83	-	≥ 0.8	NA
Initial carrier frequency tolerance		-40	+3.7	40	± 40	kHz
Carrier frequency drift rate		-20	+7.1	20	± 20	kHz/50us
Carrier frequency drift: Max Drift		50	8	-	≤50	kHz
Low Energy – Receiver Test (Channel 39_2480MHz)						
Receiver sensitivity		-	-80	-70	≤-70	dBm
Receiver sensitivity - Frame Error Rate		-	0	30.8	≤30.8	%
PER Report Integrity - Frame Error Rate		50	50	65.4	50.0 ≤ PER ≤ 65.4	%

2 Software Specification

2-1 WiFi

2-1-1 OS Support & Available Drivers

- SDIO 4-bit
  - Linux 2.4 & 2.6
  - Android
  - RTOS

2-1-2 Security Features Supported

- Support for IEEE 802.11i security enhancements
  - WEP
  - TKIP
  - AES
  - WPA
  - WPA2
  - WAPI

2-1-3 Other Features

- Host wakeup signaling
- Soft AP (for Linux and Android)
- WIFI Direct

2-2 Bluetooth Software Stacks

apm6656 is supplied with Bluetooth v4.0+EDR compliant stack firmware, which runs on internal RISC microcontroller.

2-2-1 HCI Stack

All Bluetooth v2.1+EDR mandatory and optional features are supported. The firmware also extends the standard Bluetooth functionality with numerous features. Please contact apmcomm FAE for details.

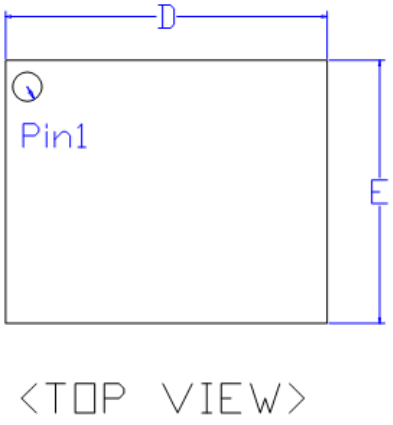
2-2-2 Host Software

BlueCore Embedded Host Software (BCHS). About the Host Software, please contact apmcomm FAE for details.

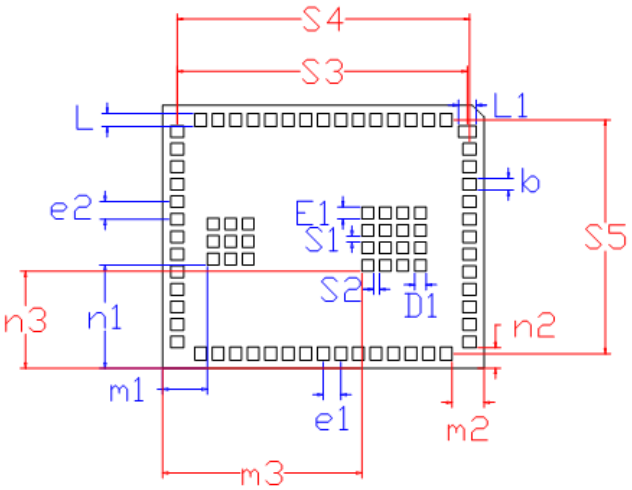
3 Mechanical Specification

Dimension	9×11×1.55 mm (max. height)
Pinout	56
Weight	0.3g
Antenna	External antenna support (Pin 53)

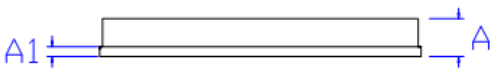
3-1 Package Outline



<TOP VIEW>



<BOTTOM VIEW>



<SIDE VIEW>

Unit:mm

Symbol	Min	Nor	Max
D	10.9	11	11.1
E	8.9	9	9.1
A	-	1.3	1.55
A1	-	0.35	0.45
m1	1.43	1.53	1.63
n1	3.44	3.54	3.64
m2	1	1.1	1.2
n2	0.6	0.7	0.8
m3	6.72	6.82	6.92
n3	3.22	3.32	3.42
e1	-	0.6	-

Symbol	Min	Nor	Max
D1	0.34	0.4	0.46
E1	0.34	0.4	0.46
L	0.39	0.45	0.51
L1	0.5	0.6	0.7
b	0.34	0.4	0.46
S1	0.15	0.2	0.25
S2	0.15	0.2	0.25
S3	9.83	9.93	10.03
S4	9.9	10	10.1
S5	7.9	8	8.1
e2	-	0.6	-

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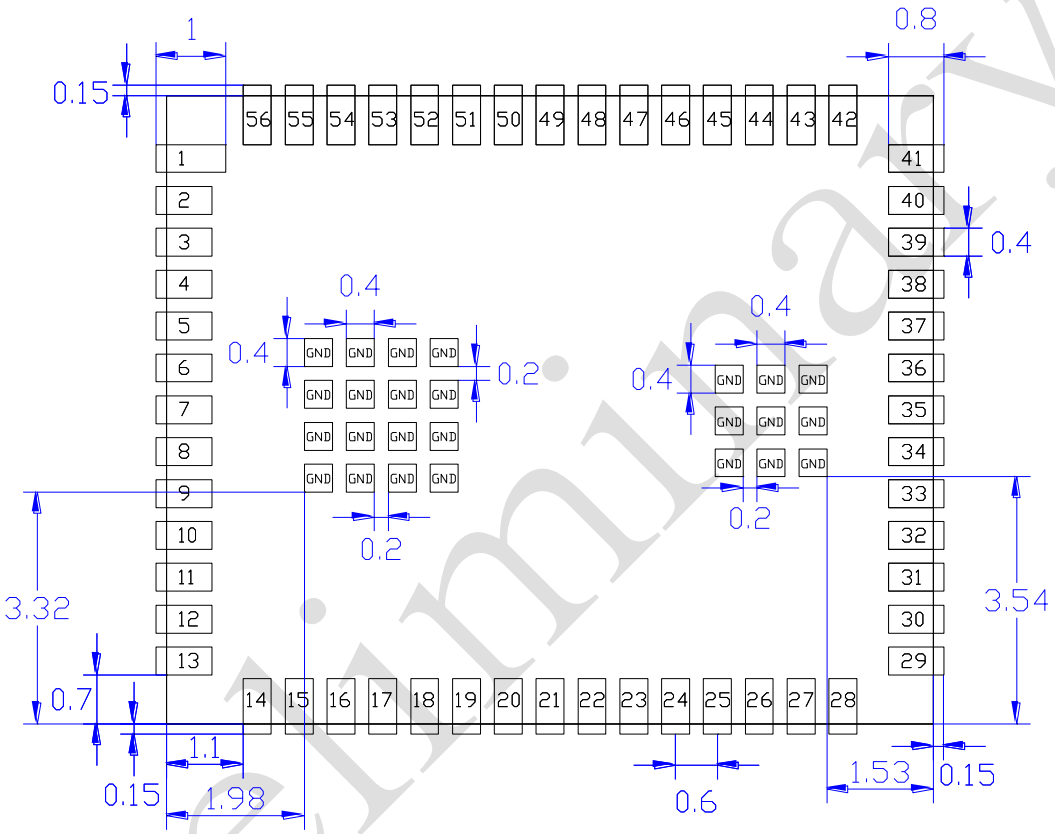
4 Assembly Guideline

4-1 Recommended Mounting Pad Design (Top View)

The following figure illustrates the recommended mounting pad design for apm6656.



TOP VIEW (mm)

4-2 Recommendation for Stencil Aperture in SMT Process

Please follow general QFN stencil design guideline. Some rules of thumb are highlighted below.

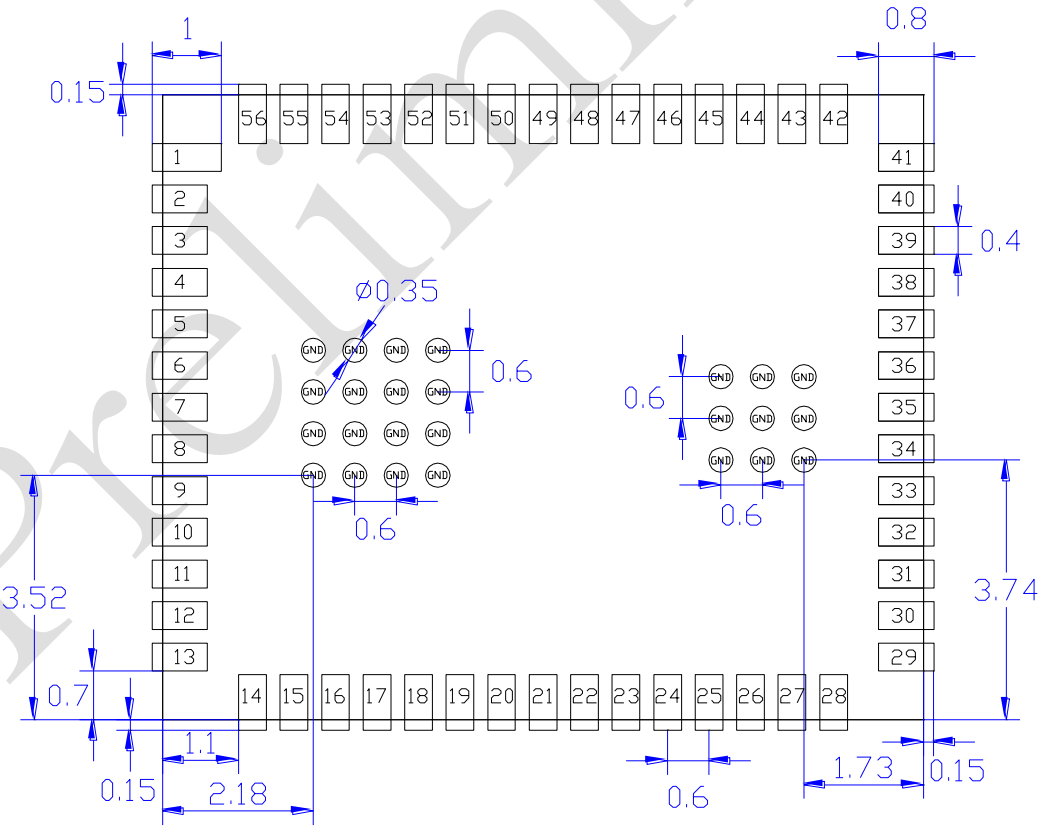
• The LGA pads should NOT be flooded over with copper, they should be connected into the plane with a track width of approx 50% of the pad width, this will mean more heat will be available at the joint. Track lengths should obviously be minimized, we would generally use about 0.3mm on external layers.

• The solder paste pattern for the internal Tab pads could be split into 4 smaller segments for the 2 large pads, and 2 smaller segments for the smaller pads, this should have the effect of preventing the paste from pooling into one area, and hence minimize the likelihood of the pads being held away from each other. We use a rule of thumb of 50% solder paste area in relation to Tab copper area (this only applies to tab pads under the device – not the signal pads).

• The thickness of the solder paste stencil has implications on solder joint quality as well, we do not have the knowledge on what stencil should be specified.

• Ensure they are using a good appropriate flux, and the correct reflow profile for unleaded (basically +20C above leaded) which is also uniform in nature.

Violating the basic rules might cause problems. For example, if the stencil apertures of the internal ground planes are improperly big, they would hold more solders in SMT process and may cause the module peripheral pads un-contacted to the main board. To improve this situation, apmcomm suggests the stencil opening shown as follows.



Stencil Aperture (Top View)

4-3 Baking condition recommendation before IR reflow

Baking condition for apm6656 module:

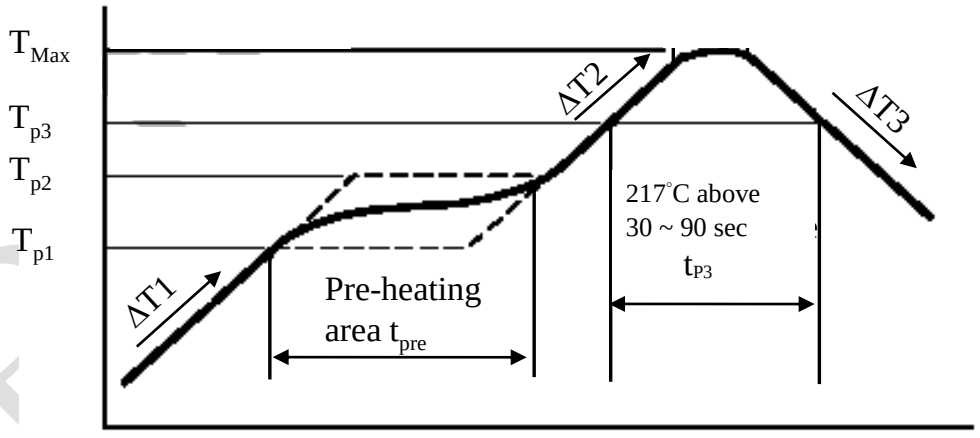
I: 125℃/4 hrs baking is necessary for apm6656 module before SMT process. After baking treatment the modules can be stored in the environment under 30℃ and 60% RH for 48 hrs. If the storage time is over 48 hrs, the modules need to be re-baked using the same condition again.

II: In the event that the sealed bag is damaged on receipt of the modules, the baking condition should be changed to 125℃/8 hrs.

4-4 Recommendation for Reflow Profile

Maximum reflow temperature is 250℃.

Preheat ramp-up rate	125℃ to 180℃ 1 to 3℃ /sec.
Peak temperature	250℃ max.
Temperature maintained above 217℃	30 ~ 90 sec.
Cooling ramp-down rate	<2℃/sec.
Maximum number of reflow cycles	≤3



Heating/Cooling Speed			Pre-Heating		Heating	
ΔT1	ΔT2	ΔT3	T_{p1}–T_{p2}	t_{pre}	T_{Max}	t_{P3}
1 to 3℃ /sec.	1 to 3℃ /sec.	< 2℃ /sec.	125 ~ 180℃	30 ~ 90 sec.	250℃ max.	30 ~ 90 sec.

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